

## IN THE CLAIMS

1           36.   (New) A host messaging unit for allowing asynchronous retrieval of a  
2   command from a host processor, the host messaging unit comprising:  
3           a read controller, coupled to a bus, for determining when a host command has been  
4   provided to a host memory and for asynchronously retrieving the host command directly from  
5   a host memory via direct memory access;  
6           a validator, coupled to the read controller, for validating the retrieved host command;  
7   and  
8           a write controller, coupled to the bus, for asynchronously signaling a successful  
9   command transfer from the host memory to the host messaging unit via direct memory  
10   access.

1           37.   (New) The host messaging unit of claim 36, wherein the read controller  
2   comprises a read clock for initiating the command retrieval from the host memory at  
3   predetermined intervals.

1           38.   (New) The host messaging unit of claim 37, wherein the read clock allows  
2   programmable predetermined intervals.

1           39.   (New) The host messaging unit of claim 38, wherein the read clock restarts  
2   the predetermined interval after the command retrieval from the host memory.

1           40.   (New) The host messaging unit of claim 37, wherein the write controller  
2   clears the host memory to inform the host that the host command has been read.

1           41.     (New) The host messaging unit of claim 36, wherein the read controller  
2     comprises a busmaster command engine for initiating the command retrieval from the host  
3     memory when the busmaster command engine receives a signaled indicating host commands  
4     are available in the host memory.

1           42.     The host messaging unit of claim 41, wherein the busmaster command engine  
2     comprises a register programmable for indicating that the command is available to be  
3     retrieved from the host memory.

1           43.     (New) A peripheral component interconnect device comprising:  
2                 a device processor; and  
3                 a host messaging unit coupled to the device processor for facilitating communication  
4     between the device processor and an external device, the host messaging unit including:  
5                 a read controller, coupled to a bus, for determining when a host command has  
6     been provided to a host memory and for asynchronously retrieving the host command directly  
7     from a host memory via direct memory access;  
8                 a validator, coupled to the read controller, for validating the retrieved host  
9     command; and  
10                a write controller, coupled to the bus, for signaling a successful command  
11     transfer from the host memory to the host messaging unit.

1           44.     (New) The host messaging unit of claim 43, wherein the read controller  
2     comprises a read clock for initiating the command retrieval from the host memory at  
3     predetermined intervals.

1           45.     (New) The host messaging unit of claim 44, wherein the read clock allows  
2     programmable predetermined intervals.

1           46.     (New) The host messaging unit of claim 45, wherein the read clock restarts  
2     the predetermined interval after the command retrieval from the host memory.

1           47.     (New) The host messaging unit of claim 44, wherein the write controller  
2     clears the host memory to inform the host that the host command has been read.

1           48.     (New) The host messaging unit of claim 43, wherein the read controller  
2     comprises a busmaster command engine for initiating the command retrieval from the host  
3     memory when the busmaster command engine receives a signaled indicating host commands  
4     are available in the host memory.

1           49.     The host messaging unit of claim 48, wherein the busmaster command engine  
2     comprises a register programmable for indicating that the command is available to be  
3     retrieved from the host memory.

1           50.     (New) A method of asynchronously servicing a peripheral component  
2     interconnect device comprising:  
3           determining when a host command has been provided to a host memory;  
4           asynchronously retrieving the host command directly from the host memory via direct  
5     memory access;  
6           validating the retrieved host command; and  
7           signaling a successful command transfer from the host memory to the host messaging  
8     unit.

1           51.     (New) The host messaging unit of claim 50, wherein the asynchronously  
2     retrieving the host command directly from the host memory via direct memory access further  
3     comprises providing a clock for initiating the retrieval of the host command from the host  
4     memory at predetermined intervals.

1           52.     (New) The host messaging unit of claim 51, wherein the signaling a  
2     successful command transfer from the host memory to the host messaging unit further  
3     comprises clearing the host memory to inform the host that the host command has been read.

1           53.     (New) The host messaging unit of claim 50, wherein the asynchronously  
2     retrieving the host command directly from the host memory via direct memory access further  
3     comprises initiating the command retrieval from the host memory upon receipt of a signal  
4     indicating host commands are available in the host memory.

1           54.     (New) An article of manufacture comprising”  
2           a program storage medium readable by a computer, the medium tangibly embodying  
3     one or more programs of instructions executable by the computer to perform operations for  
4     reducing bus transfer overhead between a host processor and a peripheral component  
5     interconnect device processor, the operations comprising:  
6           determining when a host command has been provided to a host memory;  
7           asynchronously retrieving the host command directly from the host memory via direct  
8     memory access;  
9           validating the retrieved host command; and  
10          signaling a successful command transfer from the host memory to the host messaging  
11     unit.

1           55.     (New) A peripheral component interconnect device comprising:  
2           a device processing means; and  
3           a host messaging means coupled to the device processing means for facilitating  
4     communication between the device processing means and an external device, the host  
5     messaging means including:  
6                 read control means, coupled to a bus, for determining when a host command  
7     has been provided to a host memory and for asynchronously retrieving the host command  
8     directly from a host memory via direct memory access;  
9                 validating means, coupled to the read control means, for validating the  
10    retrieved host command; and  
11                 write control means, coupled to the bus, for signaling a successful command  
12    transfer from the host memory to the host messaging unit.